CLAIMS

1. A TFT comprising a polycrystalline silicon channel (11) extending between a source (5) and drain (6), a gate (10) overlying the channel, and of a thickness to define an upstanding gate side wall (15, 16), a LDD region (12a, 12b), and a spacer (13, 14) overlying the LDD region, wherein the spacer comprises a conductive region (13a, 13b, 14a, 14b) that both overlies the LDD region and extends along the upstanding gate side wall.

2. A TFT according to claim 1 wherein the conductive region (13a, 13b, 14a, 14b) comprises a layer that is thinner than the thickness of the gate (10) and has a first portion (13b, 14b) overlying the LDD region and a second portion (13a, 14a) extending along the upstanding side wall (15, 16) of the gate.

3. A TFT according to claim 2 wherein the conductive region (13, 14) comprises a layer of conductive material.

4. A TFT according to claim 3 wherein the layer (13, 14) is a metallic layer deposited by sputtering.

5. A TFT according to claim 3 wherein the layer (13, 14) comprises a doped semiconductor material.

6. A TFT according to any one of claims 2 to 5 including a fillet (17) over the first portion of the conductive region.

7. An active plate (30) for an active matrix display, including a TFT according to any preceding claim.

8. An active matrix liquid crystal display comprising an active plate according to claim 7, a passive plate (34), and a layer of liquid crystal material (32) sandwiched between the active and passive plates.

9. A method of fabricating a polycrystalline silicon channel TFT with a gate (10) overlying its channel (11), having an upstanding gate side wall (15, 16), the method comprising the steps of:

(a) providing a gate (10) separated from a polycrystalline silicon layer (4) by an insulating layer (9);

(b) implanting a dopant into the polycrystalline silicon layer (4) using the gate (10) as a mask;

(c) forming a spacer (13, 14) after step (b) adjacent to the gate (10) that comprises a conductive region which overlies the polycrystalline silicon layer and extends along the gate side wall (15, 16); and

(d) implanting a dopant into the polycrystalline silicon layer (4) using the gate (10) and the spacer (13, 14) as a mask to form a source or drain region (5 or 6), such that the spacer (13, 14) overlies an LDD region (12a, 12b) in the polycrystalline silicon layer (4) between the source or drain region (5 or 6) and the channel (11).

10. A method according to claim 9 wherein step (c) comprises includes depositing a layer (13, 14) of conductive material over the polycrystalline silicon layer and the gate, and selectively etching the deposited layer of conductive material to form the spacer with a first portion overlying the polycrystalline silicon layer and a second portion extending along on the side wall of the gate.

11. A method according to claim 10 including depositing the layer of conductive material to a thickness which is less than that of the gate.

12. A method according to claim 10 or 11 including depositing the conductive material in a non-conformal layer.

13. A method according to any one of claims 10 to 12 including depositing the layer by sputtering.

14. A method according to any one of claims 10 to 13 including depositing said layer as a metallic layer.

15. A method according claim 10 or 11 wherein the selective etching of the conductive layer is carried out by forming a fillet (17) over the first portion thereof, and selectively etching the layer where not protected by the fillet.

16. A method according to claim 13 including depositing a further layer on said conductive layer, and selectively etching the further layer to form the fillet therefrom.

17. A method according to claim 16 including depositing the further layer as a conformal layer.

18. A method according to claim 16 including depositing the further layer as a Si containing layer.

19. A method according to any one of claims 15 to 18 including depositing the further layer by CVD.